

100

FIGURE 1A

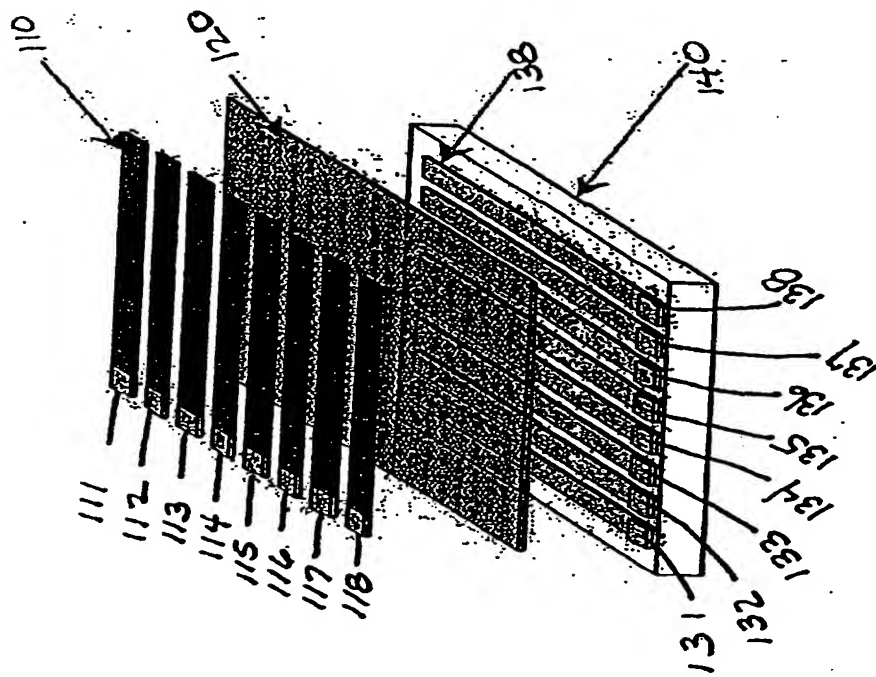


FIGURE 1B

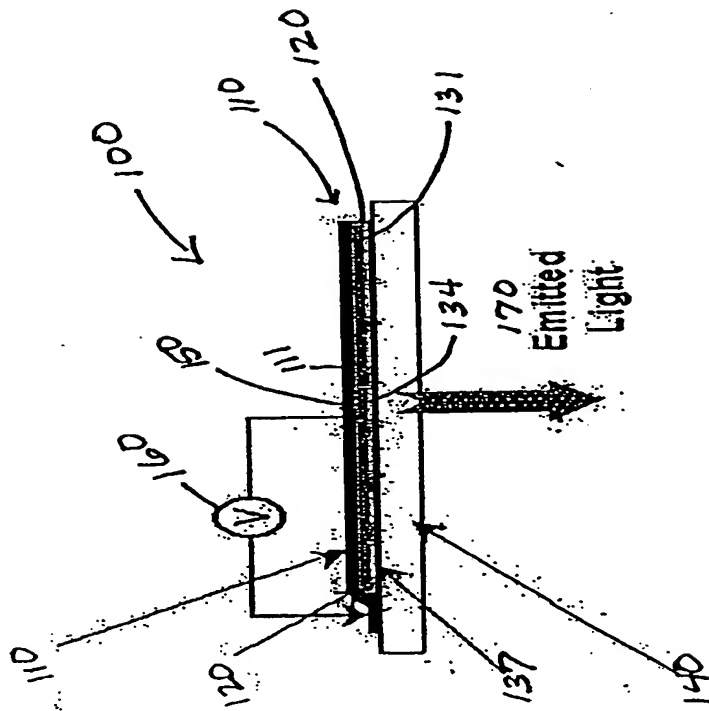
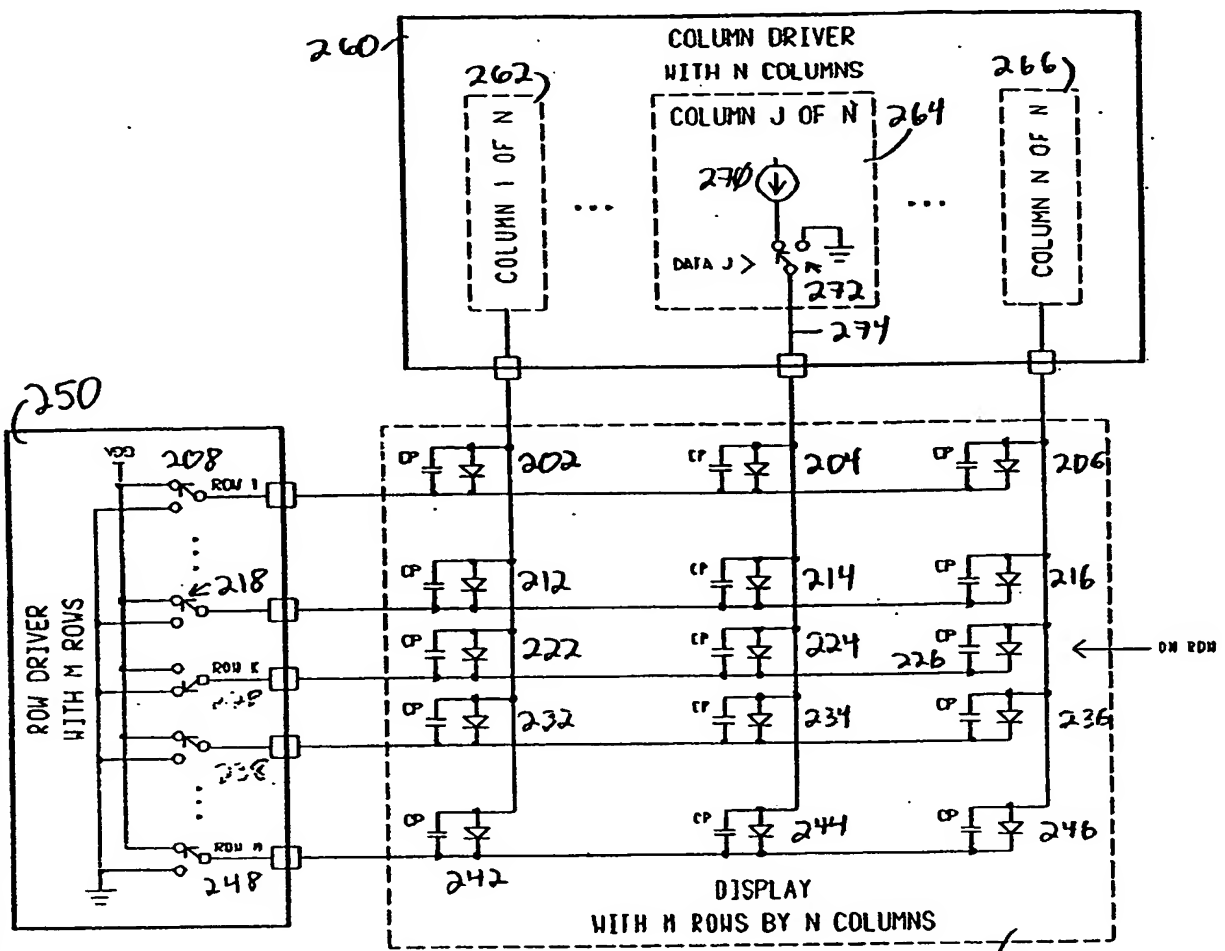


FIG. 2 is a schematic diagram of a display device 250 in accordance with the present invention. The display device 250 includes a row driver 250 and a column driver 260. The row driver 250 is connected to a display 280 and provides a row address signal to the display 280. The column driver 260 is connected to the display 280 and provides a column address signal to the display 280. The display 280 is a matrix of pixels 202, 204, 206, 212, 214, 216, 222, 224, 226, 232, 234, 236, 242, 244, 246. Each pixel 202, 204, 206, 212, 214, 216, 222, 224, 226, 232, 234, 236, 242, 244, 246 is connected to a row line 208, 218, 228, 238, 248 and a column line 262, 264, 266. The row lines 208, 218, 228, 238, 248 are connected to the row driver 250. The column lines 262, 264, 266 are connected to the column driver 260. The display 280 is a matrix of pixels 202, 204, 206, 212, 214, 216, 222, 224, 226, 232, 234, 236, 242, 244, 246. Each pixel 202, 204, 206, 212, 214, 216, 222, 224, 226, 232, 234, 236, 242, 244, 246 is connected to a row line 208, 218, 228, 238, 248 and a column line 262, 264, 266. The row lines 208, 218, 228, 238, 248 are connected to the row driver 250. The column lines 262, 264, 266 are connected to the column driver 260.



Prior Art
Figure 2

FIG. 3 is a block diagram of a digital image sensor system 300. The system includes a digital block 340 and an analog block 350. The digital block 340 contains three lookup tables: TABLE 1 (NDTV LOOKUP TABLE 364), TABLE 2 (PIXEL OFFSET COMPENSATION LOOKUP TABLE 348), and TABLE 3 (COLUMN RESISTANCE CORRECTION LOOKUP TABLE 352). It also includes a digital averaging block 356. The analog block 350 contains a column driver 304, a D/A converter 328, and a calibration circuit 354. The column driver 304 includes a channel select input Y, a left-right input, and a 1 of M channels input. The D/A converter 328 converts digital data to analog. The calibration circuit 354 includes a 1-bit D/A converter 346 and an A/D converter 352. The system also includes a channel output 308.

FIG. 3

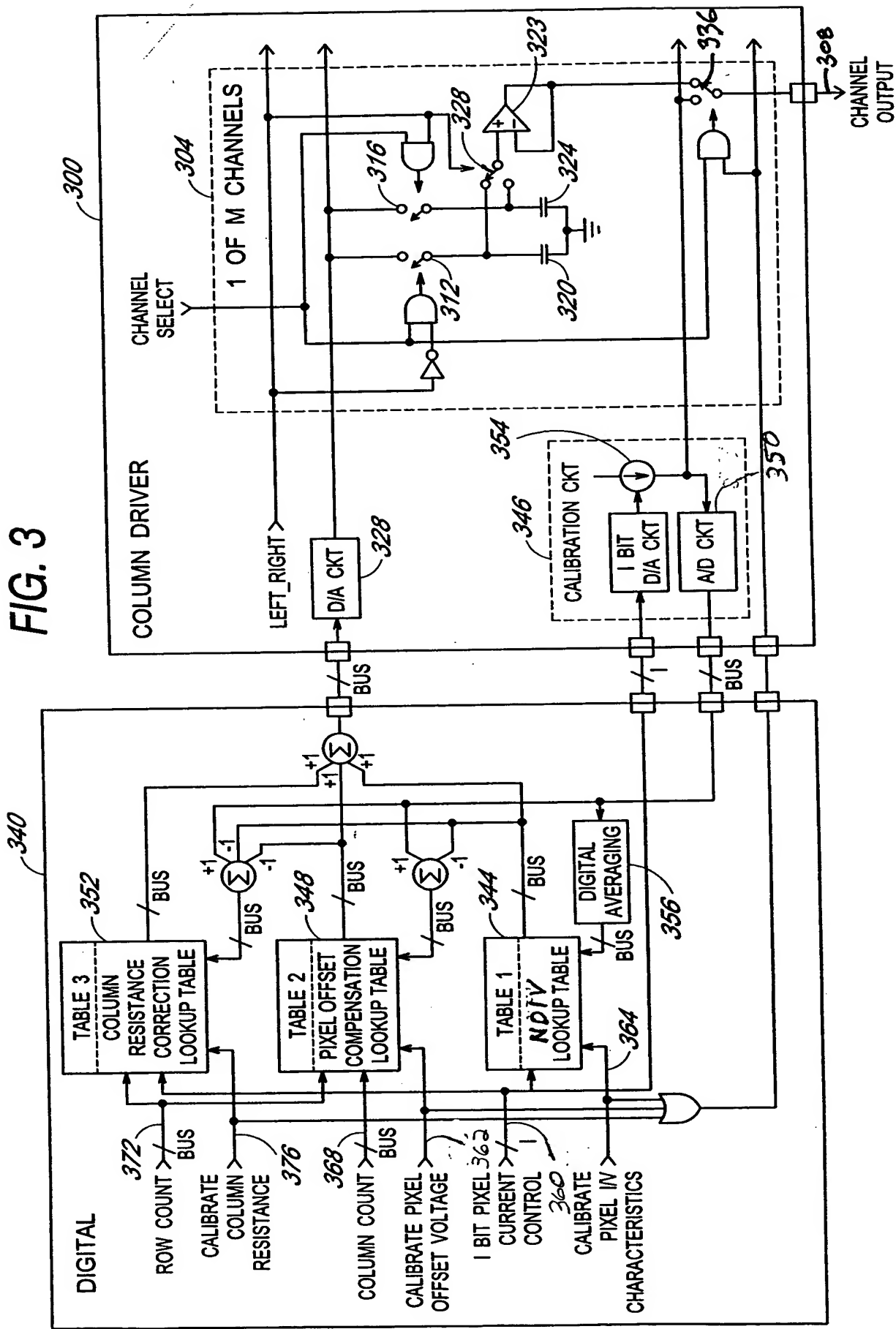
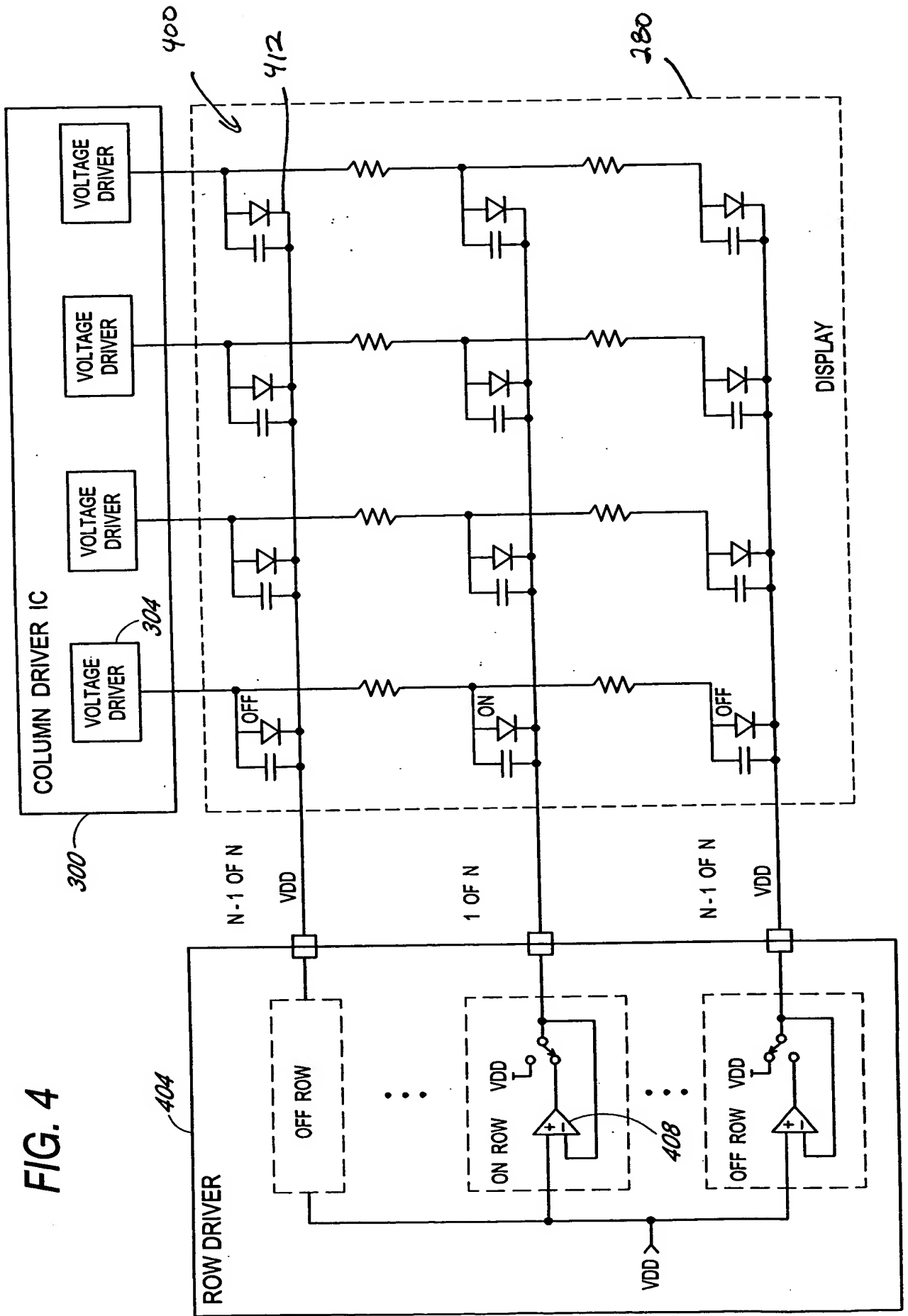


FIG. 4



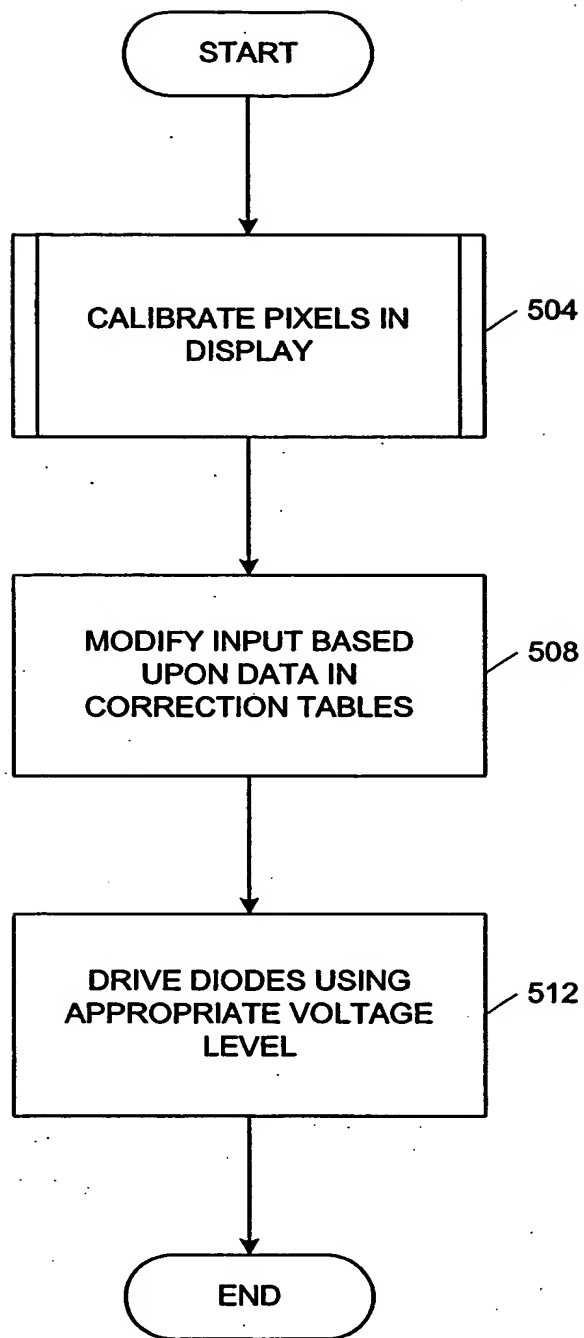


FIG. 5

504

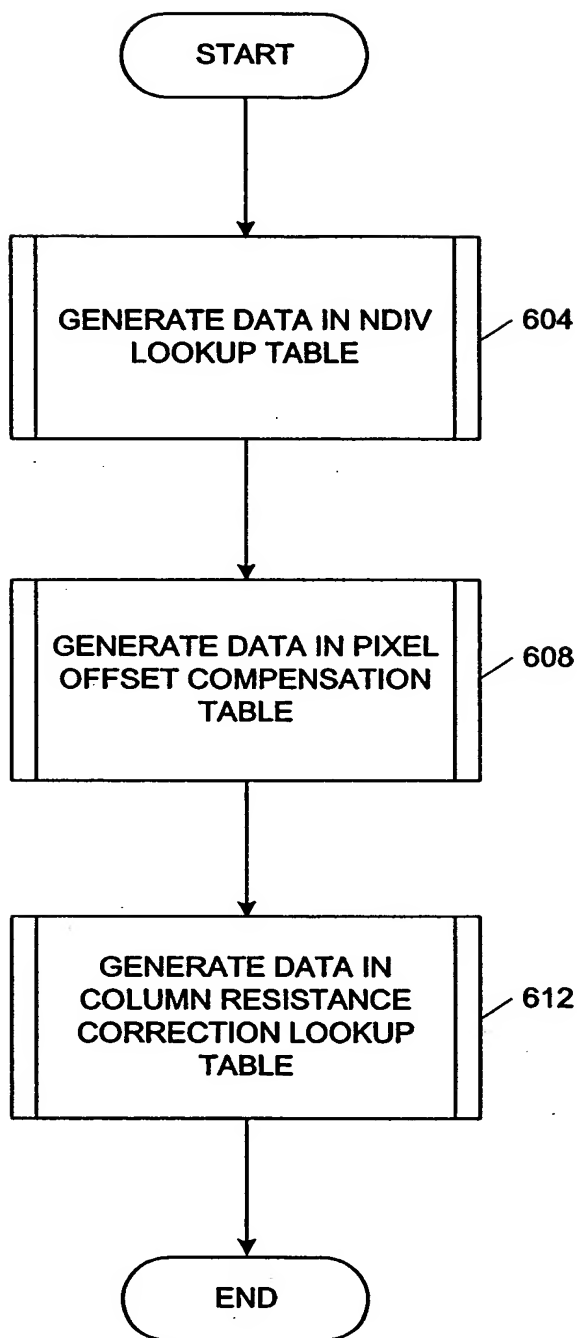


FIG. 6

604

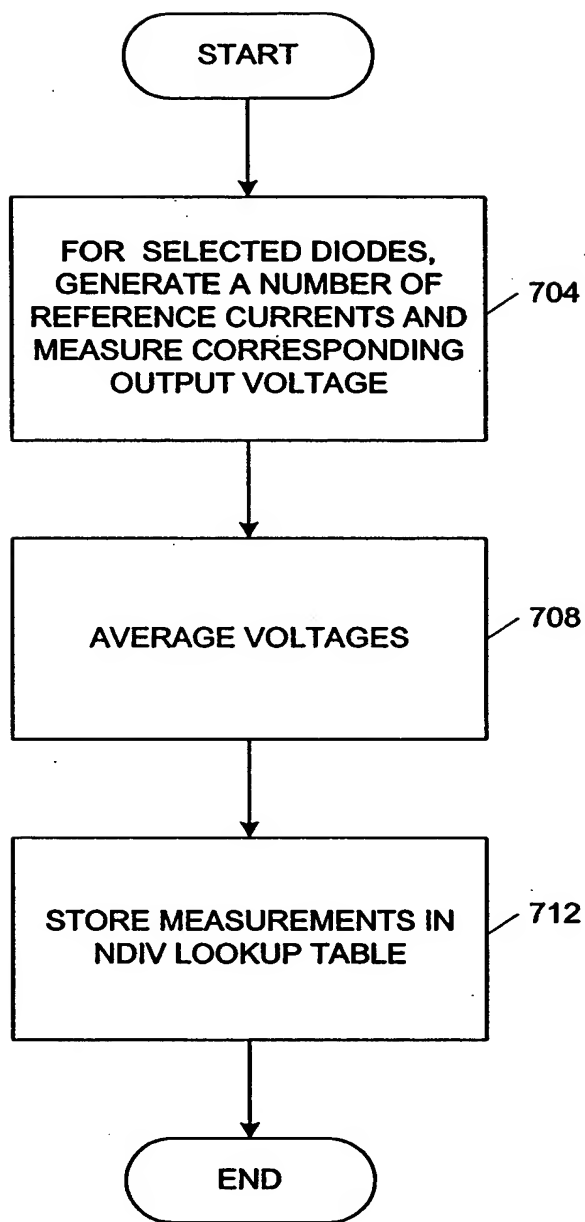


FIG. 7

608

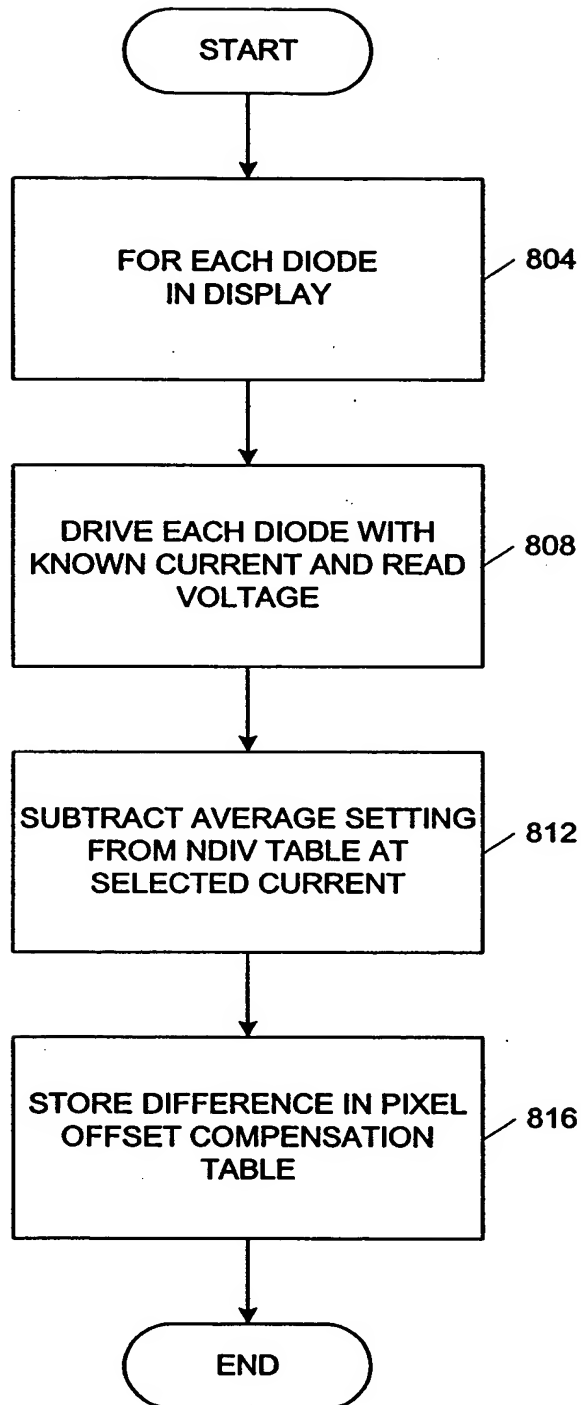


FIG. 8

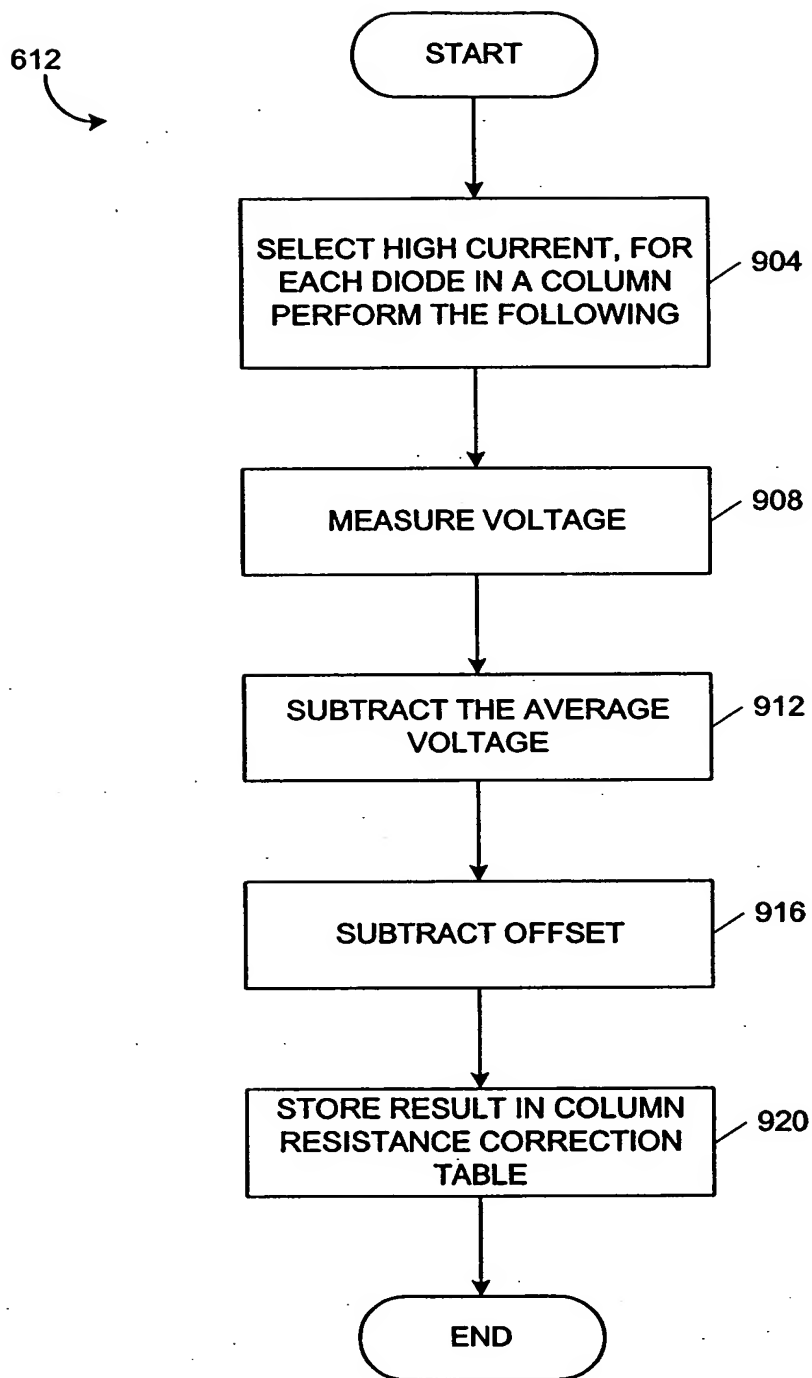


FIG. 9